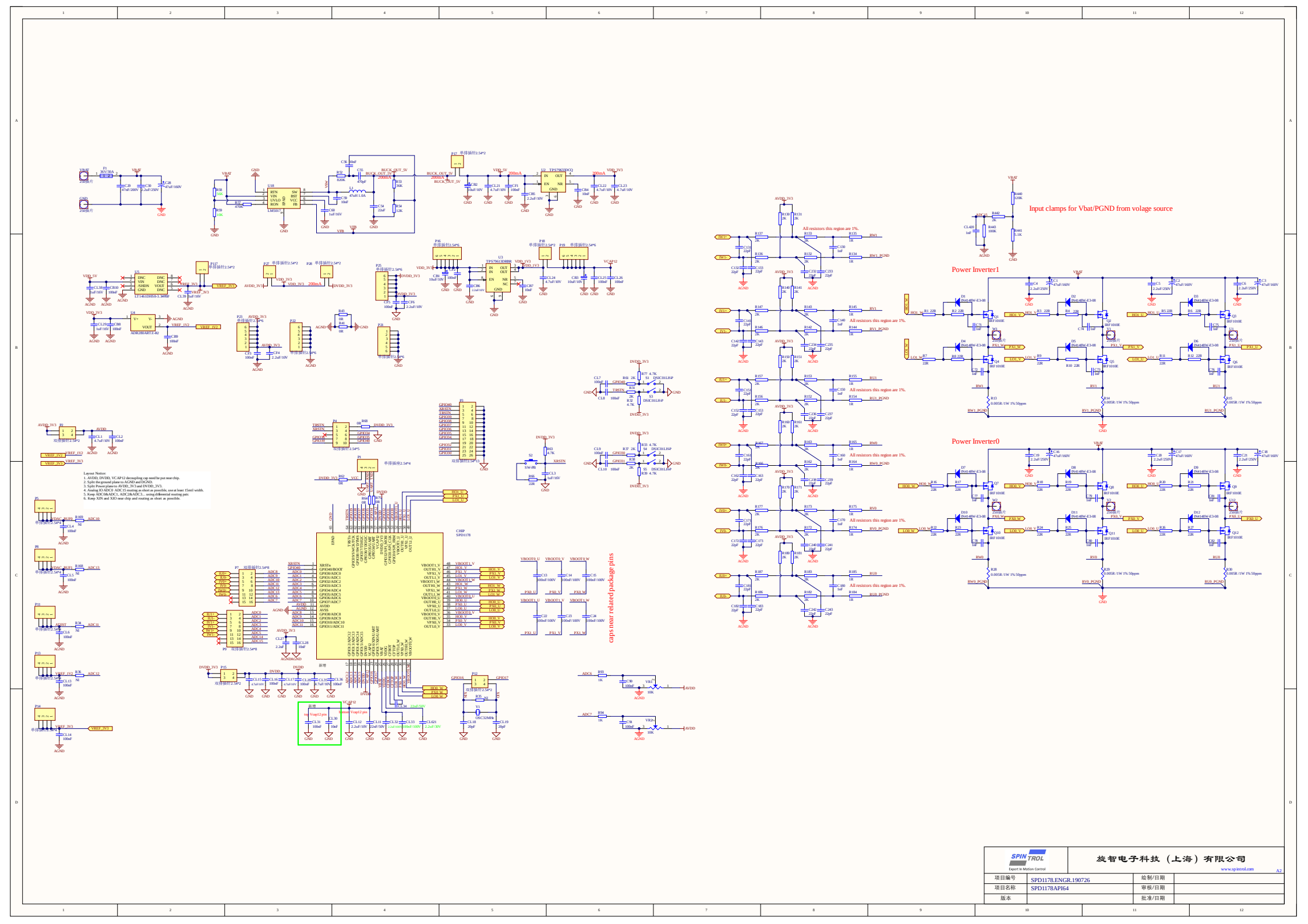
Input clamps for Vbat/PGND from volage source
Power Inverter1
Power Inverter0
All resistors this region are 1%.
caps near related package pins
Layout Notice:
1. AVDD, DVDD, VCAP12 decoupling cap need be put near chip.
2. Split the ground plane to AGND and DGND.
3. Split Power plane to AVDD_3V3 and DVDD_3V3.
4. Analog IO ADC0 ADC15 routing as short as possible, use at least 15mil width.
5. Keep ADC0&ADC1, ADC2&ADC3... using differential routing pair.
6. Keep XIN and XIO near chip and routing as short as possible.
CHIP
SPD1178
SPIN TROL
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A2
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